

IN THE CLAIMS

The following are Claims 1-19.

1. (Original) A sense amplifier circuit comprising:

a sense amplifier coupled to a first input line and a second input line and adapted to receive an enable signal, wherein the enable signal controls whether the sense amplifier is enabled;

a first inverter coupled to the first input line and adapted to provide a first output signal;

a second inverter coupled to the second input line and adapted to provide a second output signal; and

a logic gate adapted to receive the first output signal and the second output signal and to provide a trip signal.

2. (Original) The sense amplifier circuit of Claim 1, wherein the trip signal indicates when the sense amplifier has read a data value provided on the first input line and/or the second input line and when the first input line and the second input line are precharged.

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3. (Original) The sense amplifier circuit of Claim 1, further comprising a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value.

4. (Original) The sense amplifier circuit of Claim 1, further comprising:

a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value; and

a precharge circuit adapted to precharge the first input line and/or the second input line, wherein when the enable signal enables the sense amplifier, the precharge circuit stops precharging the first input line and/or the second input line.

5. (Original) The sense amplifier circuit of Claim 1, further comprising:

a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value;

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a precharge circuit adapted to precharge the first input line and/or the second input line when the enable signal transitions to a first value, with the trip signal transitioning to a second value when the first input line and/or the second input line reach precharge values; and

a column multiplexer adapted to select which data lines to couple to the first input line and/or the second input line, wherein when the enable signal enables the sense amplifier by transitioning to a second value, the precharge circuit stops precharging the first input line and/or the second input line and the column multiplexer couples at least one data line to the first input line and/or the second input line.

6. (Original) The sense amplifier circuit of Claim 5, further comprising a global precharge circuit adapted to precharge the data lines.

7. (Original) The sense amplifier circuit of Claim 1, further comprising a sense amplifier circuit controller adapted to control one or more of the sense amplifier circuits by controlling the enable signal and monitoring the trip signal of each of the sense amplifier circuits.

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8. (Original) The sense amplifier circuit of Claim 1, wherein the first and second input lines are couplable to bitlines of a memory array, wherein the memory array comprises a number of sense amplifier circuits adapted to read data stored in the memory array.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Original) A method of reading data from data lines, the method comprising:

disabling a sense amplifier coupled to the data lines;

precharging the data lines;

providing a first signal value via inverters coupled to the data lines when the data lines are precharged;

providing the data on the data lines after the first signal value is provided;

enabling the sense amplifier to read the data placed on the data lines after the first signal value is provided; and

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providing a second signal value via the inverters coupled to the data lines when the sense amplifier has read the data placed on the data lines.

15. (Original) The method of Claim 14, further comprising repeating the method by disabling the sense amplifier and precharging the data lines after the second signal value is provided.

16. (Original) The method of Claim 14, further comprising storing an output signal provided by one of the inverters when the second signal value is provided.

17. (Original) The method of Claim 14, further comprising disabling the precharging after the first signal value is provided.

18. (New) The sense amplifier circuit of Claim 1, further comprising:

a precharge circuit adapted to precharge at least one of the first input line and the second input line, wherein when the enable signal enables the sense amplifier, the precharge circuit stops precharging at least one of the first input line and the second input line; and

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a sense amplifier circuit controller adapted to control the enabling and disabling of the sense amplifier circuit and the precharge circuit based on the trip signal.

19. (New) The sense amplifier circuit of Claim 1, further comprising:

a latch adapted to store a result provided by the first output signal or the second output signal, wherein the result is stored by the latch when the trip signal transitions to a first value;

a precharge circuit adapted to precharge the first input line and/or the second input line when the enable signal transitions to a first value, with the trip signal transitioning to a second value when the first input line and/or the second input line reach precharge values; and

a column multiplexer adapted to select which data lines to couple to the first input line and/or the second input line, wherein when the enable signal enables the sense amplifier by transitioning to a second value, the precharge circuit stops precharging the first input line and/or the second input line and the column multiplexer couples at least one data line to the first input line and/or the second input line, wherein the data lines are from a memory array with the

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sense amplifier circuit adapted to read data stored in the  
memory array.

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